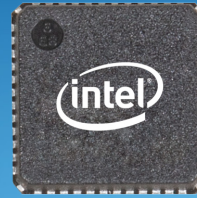


Intel® Ethernet Controller I225



PCI Express multi-gigabit Ethernet controller supporting mobile, desktop, workstation, value-server, or embedded space-constrained designs.

Key Features

- PCI Express 3.1 (5GT/s) x1 host interface
- MDI (Copper) standard IEEE 802.3 Ethernet interface up to 2.5Gb/s¹
- Time Sensitive Networking (TSN) capability support
- Innovative power management features
- Support for Intel® Active Management Technology on systems enabled with Intel vPro® technology

Overview

This PCI Express controller with Base-T copper networking interface, provides compact, single-port integrated multi-gigabit (up to 2.5G) - MDI (Copper) standard IEEE 802.3 Ethernet interface for 2500BASE-T, 1000BASE-T, 100BASE-TX, 10BASE-TE connections (IEEE 802.3, 802.3u, 802.3ab).

The Intel® Ethernet Controller I225 is designed for use on any mobile, desktop, workstation, value-server, or industrial designs that have critical space constraints. The I225 can also support Intel vPro® technology on specific Intel platforms and chipsets.

The Intel Ethernet Controller I225 also supports the latest time sensitive networking (TSN) features, along with best in class power management and Operating System Support.

Filled with Performance Optimization Capabilities

The Intel® Ethernet Connection I225 includes advanced interrupt-handling features to reduce CPU overhead. Other performance-enhancing features include offloading TCP/UDP (for both IPv4 and IPv6) checksum calculations and performing TCP segmentation.

Advanced features such as Jumbo Frame support for extra-large packets and Receive Side Scaling (RSS) are also supported. Additionally, I225 builds on prior controller solutions to add Time Sensitive Networking (TSN) features including IEEE 802.1Qbu, 802.3br, 802.1Qbv, 802.1AS-REV, 802.1p/Q, and 802.1Qav on select operating systems. These features support advanced time critical, and synchronized applications prevalent in audio/video, embedded, and industrial applications.

Advanced interrupt-handling features manage multiple interrupts simultaneously. Combining interrupt-handling features with intelligent filtering, ordering, and directing packets to specific queues and cores, enables load-balancing network traffic flows to improve throughput in multi-core platforms.

Other performance-enhancing features include IPv4 and IPv6 checksum offload, TCP/UDP checksum offload, extended Tx descriptors for more offload capabilities, up to 256 KB TCP segmentation (TSO v2), 40 KB packet buffer size, and 9.5 KB Jumbo Frame support.

Other Advanced Features

Flexible Filters

Supports a total of 32 individually configurable flexible filters. Filters can be used for wake-up or proxying when in D3 state or for queueing when in D0 state.

Secure Flexible Firmware Architecture

Flexible Firmware Architecture with Secure NVM Update protects the flash from external unauthorized software programming. The Intel® Ethernet Controller I225 also supports Dynamic Firmware Updating that enables Firmware Updates without the need for a system reboot.

Software Definable Pins

Four Software Definable Pins (SDPs) enable additional design customization for embedded platforms. SDPs can be used for IEEE 1588 auxiliary device connections, to enable/disable the device, and for other miscellaneous hardware or software-control purposes. These pins can be individually configured to act as either standard inputs, General-Purpose Interrupt (GPI) input or output pins, as well as the default value of all pins configured as outputs. One SDP is dedicated, and three are shared with the JTAG interface.

Energy Efficient Ethernet (EEE)

Supports the IEEE 802.3az EEE standard. During periods of low network activity, EEE reduces the power consumption of an Ethernet connection by negotiating with the switch port to transition to a low power idle (LPI) state.

This capability reduces power dramatically, saving power on both the network and the switch ports. When increased traffic is detected, the controller and the switch quickly come back to full power to handle the increased traffic. EEE is supported for 2500BASE-T, 1000BASE-T and 100BASE-TX.

Flexible Design Configurations

The I225 can be used for server system configurations such as rack-mounted or pedestal servers, in an add-on NIC, and in LAN on Motherboard (LOM) designs.

- Intel Ethernet Controller I225-V/LM supports commercial temperature ranges of 0 °C to 70 °C up to 2500BASE-T.
- Intel Ethernet Controller I225-IT supports extended temperatures for embedded applications with commercial temperature ranges of -40 °C to 70 °C up to 2500BASE-T and -40 °C to 85 °C up to 1000BASE-T.

Manageability Support

The Intel® Ethernet Controller I225 provides Intel® Active Management Technology support when connected to a system with Intel vPro technology, directly as LAN on motherboard, or via a Thunderbolt device.

| FEATURES | DESCRIPTION |
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|----------|-------------|

EXTERNAL INTERFACES

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|--------------------|---|
| PCI Express 3.1 | <ul style="list-style-type: none"> • 5GT/s Support for x1 width (Lane). |
| Network Interfaces | <ul style="list-style-type: none"> • Integrated MAC + BASE-T PHY. • MDI (Copper) standard IEEE 802.3 Ethernet interface for 2500BASE-T, 1000BASE-T, 100BASE-TX, and 10BASE-TE applications (802.3, 802.3u, 802.3bz, and 802.3ab). |
| MDI Lane Swap | <ul style="list-style-type: none"> • A simple hardware strapping option that allows the ability to swap the MDI pairs order between ABCD<->DCBA. This reduces routing complexity and risk. |

BOM COST Optimization

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| On-chip integrated Switched Voltage Regulator (iSVR) | <ul style="list-style-type: none"> • Removes need for a higher cost on-board voltage regulator. |
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ETHERNET FEATURES

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|---|---|
| IEEE 802.3 auto-negotiator | <ul style="list-style-type: none"> • Automatic link configuration for speed duplex and flow control. |
| IEEE 802.3x and IEEE 802.3z compliant flow control support with software-controllable Rx thresholds and Tx pause frames | <ul style="list-style-type: none"> • Local control of network congestion levels. |
| Automatic cross-over detection function (MDI/ MDI-X) | <ul style="list-style-type: none"> • Frame loss reduced from receive overruns. |
| IEEE 1588 protocol and 802.1AS implementation | <ul style="list-style-type: none"> • Time-stamping and synchronization of time sensitive applications. • Distribute common time to media devices. |
| Supporting Time Sensitive Networking (TSN) Capabilities | <ul style="list-style-type: none"> • IEEE 802.1Qbu, 802.3br, 802.1Qbv, 802.1AS-REV, 802.1p,Q, and 802.1Qav. • Supports Time-based transmission. • Any Tx and Rx queues can be used for scheduled traffic or best effort traffic. • Supports Forwarding and Queuing Enhancements for Time-Sensitive Streams. |

POWER MANAGEMENT FEATURES

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| Controller is designed for low power consumption | <ul style="list-style-type: none"> • 2W S0-Max 2500BASE-T Active 70 °C (Intel® Ethernet Controller I225-V/LM). • 1.3W S0-Typical 2500BASE-T Active 25 °C (Intel® Ethernet Controller I225-V/LM). • 950W S0-Typical 1000BASE-T Active 25 °C (Intel® Ethernet Controller I225-V/LM). • <5mW Disconnected (Intel® Ethernet Controller I225-V/LM). |
| IEEE 802.3az - Energy Efficient Ethernet (EEE) | <ul style="list-style-type: none"> • Power consumption by the PHY is reduced; link transitions to low power Idle (LPI) state as defined in the IEEE 802.3az (EEE) standard. |
| Smart Power Down (SPD) at S0 no link/Sx no link | <ul style="list-style-type: none"> • PHY powers down circuits and clocks that are not required for detection of link activity. |
| Active State Power Management (ASPM) | <ul style="list-style-type: none"> • Optionality Compliance bit enables ASPM or runs ASPM compliance tests to support entry to L0s. |
| Full wake up support | <ul style="list-style-type: none"> • Advanced Power Management (APM) Support—[formerly Wake on LAN. <ul style="list-style-type: none"> - APM: Designed to receive a broadcast or unicast packet with an explicit data pattern (Magic Packet) and assert a signal to wake up the system. • Advanced Configuration and Power Interface (ACPI) specification v2.0c. <ul style="list-style-type: none"> - ACPI: PCIe power management based wake-up that can generate system wake-up events from a number of sources. |
| ACPI register set and power down functionality supporting D0 and D3 states | <ul style="list-style-type: none"> • Power-managed speed control lowers link speed/power when highest link performance is not required. |
| MAC Power Management controls | <ul style="list-style-type: none"> • Power management controls in the MAC /PHY enable the device to enter a low-power state. |
| Power Management Protocol Offload (Proxying) | <ul style="list-style-type: none"> • Enables the system to remain at low system power state while the NIC handles predefined ping or keep alive messages. |
| Latency Tolerance Reporting (LTR) | <ul style="list-style-type: none"> • Reports service latency requirements for memory reads and writes to the Root Complex. |

STATELESS OFFLOADS AND PERFORMANCE FEATURES

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| TCP/UDP, IPv4 checksum offloads (Rx/ Tx); | <ul style="list-style-type: none"> • Offloading capabilities and improved CPU usage. • Extended Tx descriptors. • Checksum and segmentation capability extended to new standard packet type. |
| Transmit Segmentation Offloading (TSO) (IPv4, IPv6) | <ul style="list-style-type: none"> • Increased throughput and lower processor usage. |
| Interrupt throttling control | <ul style="list-style-type: none"> • Limits maximum interrupt rate and improves CPU usage. |
| Low-Latency Interrupts | <ul style="list-style-type: none"> • Based on the sensitivity of the incoming data, the controller can bypass the automatic moderation of time intervals between the interrupts. |
| Legacy and Message Signal Interrupt (MSI) | <ul style="list-style-type: none"> • Interrupt mapping. |
| Message Signal Interrupt Extension (MSI-X) | <ul style="list-style-type: none"> • Dynamic allocation of up to 5 vectors per port. |
| Receive Side Scaling (RSS) for Windows | <ul style="list-style-type: none"> • Up to four queues per port. |
| Scalable I/O for Linux environments (IPv4, IPv6, TCP/UDP) | <ul style="list-style-type: none"> • Improves the system performance related to handling of network data on multiprocessor systems. |
| Support for packets up to 9.5 KB (Jumbo Frames) | <ul style="list-style-type: none"> • Enables faster and more accurate throughput of data. |
| PCIe v3.1 support | <ul style="list-style-type: none"> • Includes additions to PCIe to support low power link states. |
| Descriptor ring management hardware for Transmit and Receive | <ul style="list-style-type: none"> • Optimized descriptor fetch and write-back for efficient system memory and PCIe bandwidth usage. |